AMENDMENTS TO THE CLAIMS:

1. (previously presented) An information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion (11) by pipeline processing, comprising:

an instruction reading request portion (17) which assigns a read address to said instruction store portion;

an instruction buffering portion (12) including a plurality of instruction buffers (e-1, e-2) which buffer instruction sequences read from said instruction store portion;

an instruction execution unit (20) which decodes and executes instructions buffered by said instruction buffering portion (12);

a branching instruction detection portion (14) which detects a branching instruction inside the instruction sequences read from said instruction store portion; and

a branch target address information buffering portion (15) including at least first and second branch target address information buffers (b-1, b-2) which, when said branching instruction detection portion has detected a branching instruction, buffer a branch target address information for generating a branch target address of said branching instruction;

wherein:

when said branching instruction detection portion (14) detects a first branching instruction (02) in a first instruction sequence being processed (C1) which is stored in one of said plurality of instruction buffers (e-1), a branch target instruction sequence (C2) of said first branching instruction (02) is stored in the other one of said plurality of instruction buffers (e-2), and said first instruction sequence (C1) and said branch target instruction sequence (C2) are fetched from said instruction store portion (11) and stored in said plurality of instruction buffers (e-1, e-2) sequentially,

when said branching instruction detection portion (14) detects a next branching instruction (04) following the first branching instruction (02) in said first instruction sequence (C1), a first branch target address information (41) of the next branching instruction (04) is stored in the first branch target address information buffer (b-1) without prefetching a branch target instruction sequence of the next branching instruction,

when said branching instruction detection portion (14) detects a second branching instruction (12) in said branch target instruction sequence (C2), a second branch target address information (21) of the second branching instruction (12) is stored in the second branch target address information buffer (b-2) without prefetching a branch target instruction sequence of the second branching instruction, and

when said first branching instruction is executed, depending on the execution result of the first branching instruction, said branch target address information in either the first or second branch target address information buffer (b-1, b-2) is invalidated and another branch target instruction sequence starts to be fetched and stored in said instruction buffer, which is invalidated, based on the branch target address information which is not invalidated.

2. (previously presented) An information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion by pipeline processing, comprising:

an instruction reading request portion which assigns a read address to said instruction store portion;

an instruction buffering portion including first and second instruction buffers which buffer instruction sequences read from said instruction store portion;

an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion;

a branching instruction detection portion which detects a branching instruction inside the instruction sequences read from said instruction store portion; and

a branch target address information buffering portion including first and second branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer a branch target address information for generating a branch target address of said branching instruction;

wherein:

a first instruction sequence (C1) being processed is stored in either one of the first or second instruction buffers (e-1) and when said branching instruction detection portion detects a branching instruction (02) inside said first instruction sequence (C1), a second instruction sequence (C2) of the branch target of the branching instruction is stored in the other one of the first or second instruction buffers (e-2) in accordance with the branch target address information of said branching instruction (02);

the branch target address information (41) of a next branching instruction (04) inside said first instruction sequence (C1) is stored in either one of the first or second branch target address information buffers (b-1) without prefetching a branch target instruction sequence of the next branching instruction (04);

the branch target address information (21) of a branching instruction (12) inside said second instruction sequence (C2) is stored in the other one of said first or second branch target address information buffers (b-2) without prefetching a branch target instruction sequence of the branching instruction (12); and

the first or second branch target address information buffer is selected based on an execution result of the branching instruction (02) inside said first instruction sequence (C1).

3. (previously presented) The information processing device as claimed in Claim 2 wherein, in a state in which said first instruction sequence being processed (C1) is stored in either one of said first or second instruction buffers (e-1), the second instruction sequence (C2) of the branch target of the branching instruction (02) inside said first instruction sequence is stored in the other one of said first or second instruction buffers (e-2), the branch target address information (41) of the next branching instruction (04) inside said first instruction sequence (C1) is stored in said first branch target address information buffer (b-1) and the branch target address information ~~(12)~~ (21) of the branching instruction (12) inside said second instruction sequence (C2) is stored in said second branching address information buffer (b-2);

if the execution of the branching instruction (02) inside said first instruction sequence (C1) has resulted in branching, said first instruction sequence (C1) and the branch target address information of the next branching instruction (04) inside said first instruction sequence (C1) are invalidated, a third instruction sequence (C4) of the branch target of the branching instruction (12) inside said second instruction sequence (C2) is stored in one of said first or second instruction buffers (e-1), in accordance with the branch target address information which has been stored in the other one of said first or second branch target address information buffers (b-2), and the branch target address information of the next branching instruction (14) inside said second instruction sequence (C2) is stored in one of the first or second branch target address information buffers (b-1), and the branch target address information of the branching instruction

(22) inside said third instruction sequence (C4) is stored in the other one of said first or second branch target address information buffers (b-2).

4. (currently amended) The information processing device as claimed in claim 2 wherein, in a state in which said first instruction sequence being processed is stored in either one of said first or second instruction buffers, the second instruction sequence (C2) of the branch target of the branching instruction (02) inside said first instruction sequence (C1) is stored in the other one of said first or second instruction buffers, the branch target address information of the next branching instruction (04) inside said first instruction sequence (C1) is stored in said first branch target address information buffer and the branch target address information of the branching instruction (12) inside said second instruction sequence (C2) is stored in said second branching address information buffer;

if the execution of the branching instruction (02) inside said first instruction sequence (C1) has not resulted in branching, said second instruction sequence (C2) and the branch target address information of the branching instruction (12) inside said second instruction sequence (C2) are invalidated;

a fourth instruction sequence (C3) of the branch target of the next branching instruction (04) inside said first instruction sequence (C1) is stored in one of said first or second instruction buffers, in accordance with the branch target address information which has been stored in the other one of said first or second branch target address information buffers; and

a branch target address information of a further next branching instruction inside said first instruction sequence (C1) is stored in one of said first or second branch target address information buffers, and the branching address information of the branching instruction inside

said fourth branching instruction sequence (C3) is stored in the other one of said first or second branch target address information buffers.

5. (original) The information processing device as claimed in claim 1 wherein, in response to a single instruction read request from said instruction reading request portion, a plurality of consecutive instructions from said read address are read from said instruction store portion and buffered in said instruction buffering portion.

6. (previously presented) An information processing device which reads, buffers, decodes and executes instructions from an instruction store portion by pipeline processing, comprising:

an instruction reading request portion which assigns a read address to said instruction store portion;

an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said store portion;

an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion;

a branching instruction detection portion which detects a branching instruction inside the instruction sequences read from said instruction store portion, and detects branching prediction information of the branching instruction; and

a branch target address information buffering portion including a plurality of branch target address information buffers which, when said instruction detection portion has detected a branching instruction, buffers branch target address information for generating the branch target address of said branching instruction;

wherein:

when said branching instruction detection portion (14) detects a first branching instruction (02) in a first instruction sequence being processed (C1) which is stored in one of said plurality of instruction buffers (e-1), a branch target instruction sequence (C2) of said first branching instruction (02) is stored in the other one of said plurality of instruction buffers (e-2), and said first instruction sequence (C1) and said branch target instruction sequence (C2) are fetched from said instruction store portion (11) and stored in said plurality of instruction buffers (e-1, e-2) sequentially,

when said branching instruction detection portion (14) detects a next branching instruction (04) following the first branching instruction (02) in said first instruction sequence (C1), a first branch target address information (41) of the next branching instruction (04) is stored in the first branch target address information buffer (b-1) without prefetching a branch target instruction sequence of the next branching instructions,

when said branching instruction detection portion (14) detects a second branching instruction (12) in said branch target instruction sequence (C2), a second branch target address information (21) of the second branching instruction (12) is stored in the second branch target address information buffer (b-2) without prefetching a branch target instruction sequence of the second branching instructions, and

when said first branching instruction is executed, depending on the execution result of the first branching instruction, said branch target address information in either the first or second branch target address information buffer (b-1, b-2) is invalidated and another branch target instruction sequence starts to be fetched and stored in said instruction buffer, which is invalidated, based on the branch target address information which is not invalidated.

7. (previously presented) The information processing device as claimed in claim 6 wherein, whether said branch target address information buffering portion buffers the branch target address information of a branching instruction is determined in accordance with the branching prediction information of said branching instruction which is detected by said instruction detection portion.

8. (currently amended) The information processing device as claimed in claim 6 wherein, whether said instruction buffering portion fetches the first and second branch target instruction sequences ~~sequence~~ of said branching instruction is determined in accordance with the respective branching prediction information of the first and second branching instructions ~~instruction~~ which is detected by said instruction detection portion.

9. (currently amended) The information processing device as claimed in claim 6 wherein, if said branching instruction detection portion predicts with a prescribed high level of probability that the first and second branching instructions ~~instruction~~ will not branch, said branch target address information buffering portion does not fetch the branch target instruction sequence of said first and second branching instructions ~~instruction~~, respectively.

10. (original) The information processing device as claimed in claim 6 wherein, when said branch target address information buffering portion has buffered branch target address information of a first branching instruction, if said branching instruction detection portion has detected a second branching instruction which has a greater possibility of branching than said

first branching instruction, said branch target address information buffering portion invalidates the branch target address information of said first branching instruction and buffers the branch target address information of said second branching instruction.

11. (previously presented) The information processing device as claimed in claim 6 wherein, when one of said instruction buffers of said instruction buffering portion is empty, if a first branching instruction having a first branching possibility is detected by said branching instruction detection portion, a branch target instruction sequence of said first branching instruction is not fetched to said instruction buffering portion and said branching target address information buffering portion buffers the branch target address information of the first branching instruction, and if said branching instruction detection portion has detected a second branching instruction which has a second branching possibility which is higher than said first branching possibility, a branch target instruction sequence of said second branching instruction is fetched to said instruction buffering portion.

12-18. (canceled)